FIG. 1

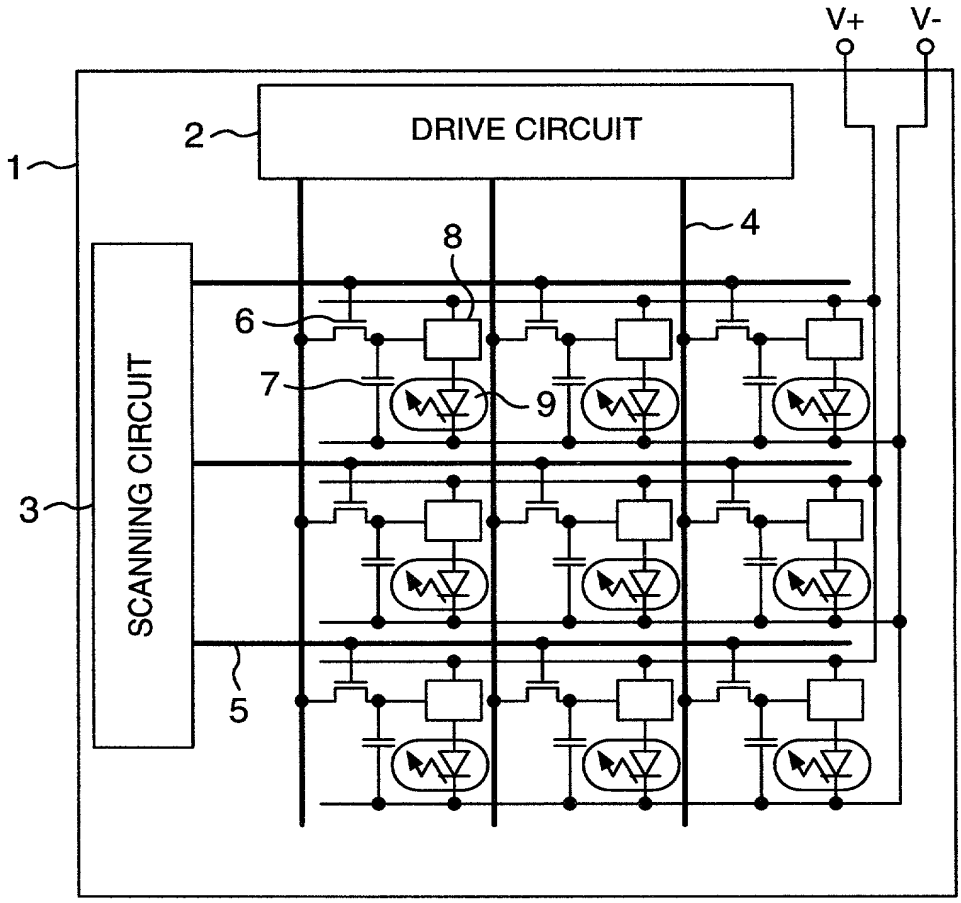
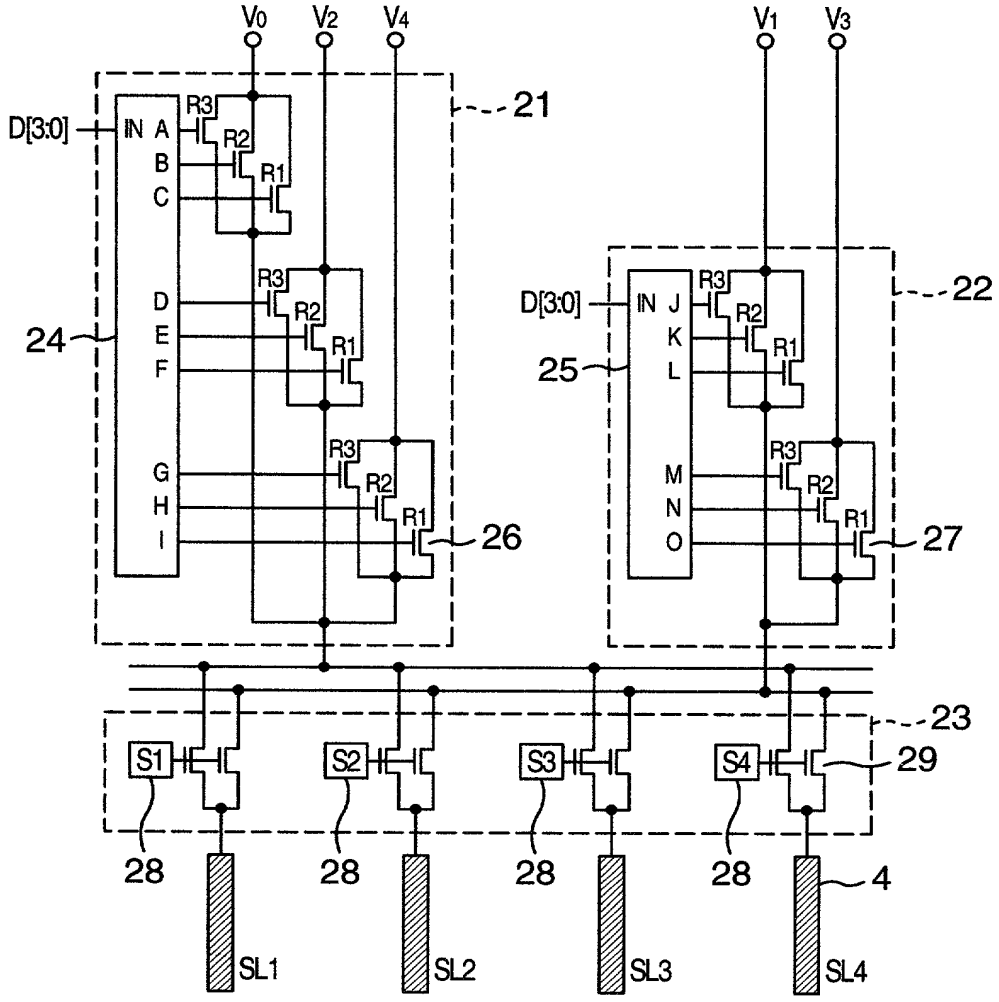


FIG. 2



21, 22 D/A CONVERSION CIRCUIT
23 SAMPLING CIRCUIT
24, 25, 28 CONTROL CIRCUIT
26, 27, 29 THIN-FILM TRANSISTOR
SL1 TO SL4 SIGNAL LINE

FIG. 3A

IN	A	B	C	D	E	F	G	H	I
0	1	1	1	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0
2	0	1	0	0	0	0	0	0	0
3	1	0	0	0	0	0	0	0	0
4	0	0	0	0	0	0	0	0	0
5	0	0	0	1	1	0	0	0	0
6	0	0	0	0	0	0	0	0	0
7	0	0	0	0	0	1	0	0	0
8	0	0	0	1	1	1	0	0	0
9	0	0	0	0	0	1	0	0	0
10	0	0	0	0	0	0	0	0	0
11	0	0	0	1	1	0	0	0	0
12	0	0	0	0	0	0	0	0	0
13	0	0	0	0	0	0	1	0	0
14	0	0	0	0	0	0	0	1	0
15	0	0	0	0	0	0	0	0	1

FIG. 3B

IN	J	K	L	M	N	O
0	0	0	0	0	0	0
1	1	0	0	0	0	0
2	0	1	0	0	0	0
3	0	0	1	0	0	0
4	1	1	1	0	0	0
5	0	0	1	0	0	0
6	0	1	0	0	0	0
7	1	0	0	0	0	0
8	0	0	0	0	0	0
9	0	0	0	1	0	0
10	0	0	0	0	1	0
11	0	0	0	0	0	1
12	0	0	0	1	1	1
13	0	0	0	0	0	1
14	0	0	0	0	1	0
15	0	0	0	1	0	0

FIG. 4

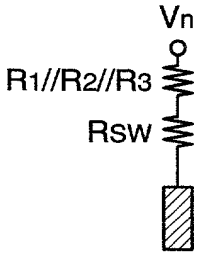
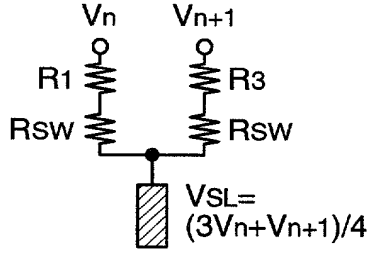
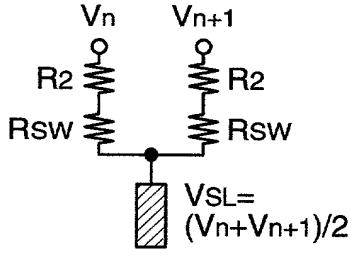
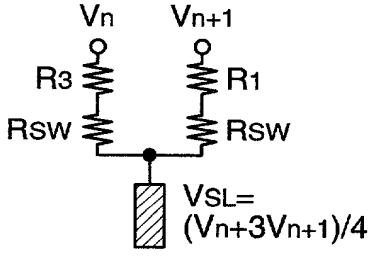
IN	GENERATION OF V_{SL}
0	
1	
2	
3	

FIG. 5

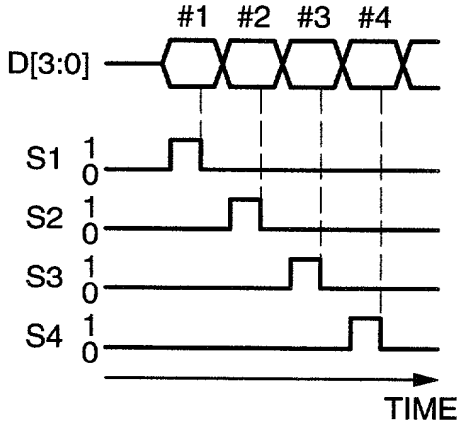


FIG. 6

D[3:0]	V_{SL}
0	V_0
1	$(3V_0+V_1)/4$
2	$(V_0+V_1)/2$
3	$(V_0+3V_1)/4$
4	V_1
5	$(3V_1+V_2)/4$
6	$(V_1+V_2)/2$
7	$(V_1+3V_2)/4$
8	V_2
9	$(3V_2+V_3)/4$
10	$(V_2+V_3)/2$
11	$(V_2+3V_3)/4$
12	V_3
13	$(3V_3+V_4)/4$
14	$(V_3+V_4)/2$
15	$(V_3+3V_4)/4$

FIG. 7

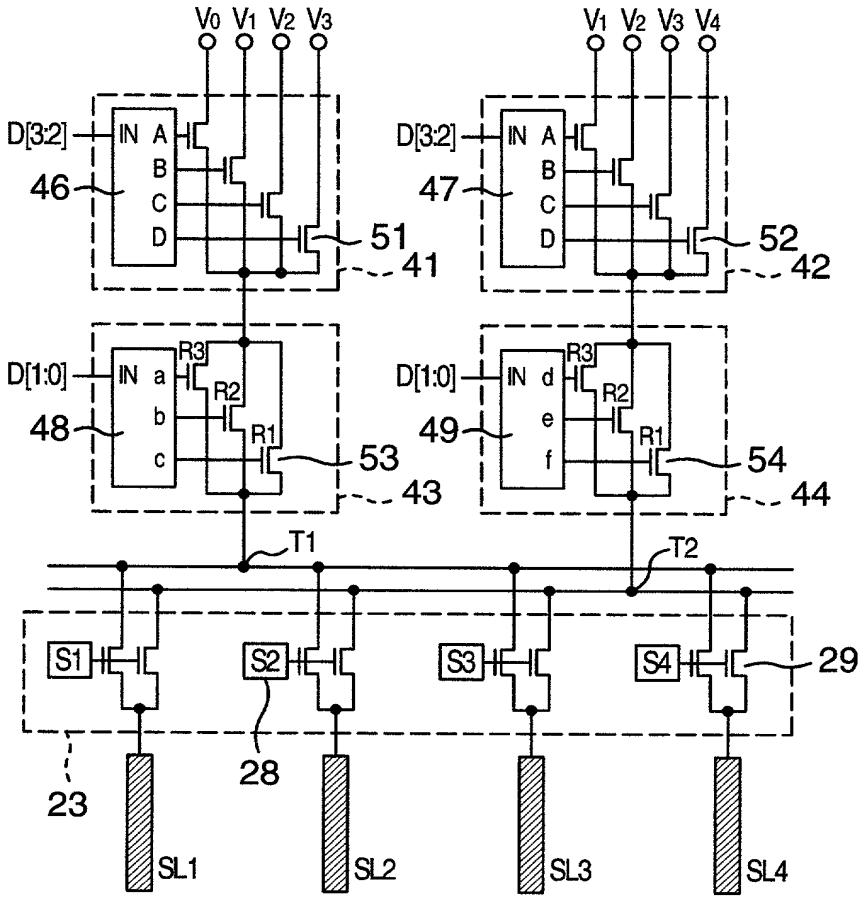


FIG. 8A

IN	A	B	C	D
0	1	0	0	0
1	0	1	0	0
2	0	0	1	0
3	0	0	0	1

FIG. 8B

IN	a	b	c
0	1	1	1
1	0	0	1
2	0	1	0
3	1	0	0

FIG. 8C

IN	d	e	f
0	0	0	0
1	1	0	0
2	0	1	0
3	0	0	1

FIG. 9

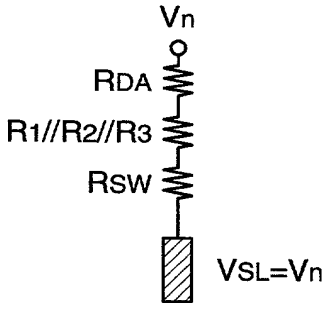
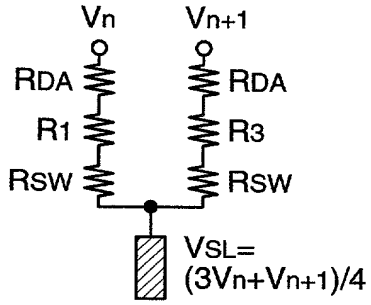
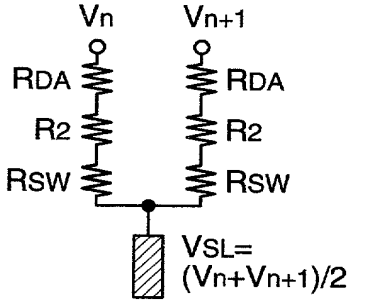
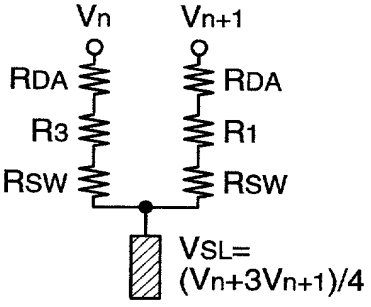
IN	GENERATION OF VSL
0	
1	
2	
3	

FIG. 10

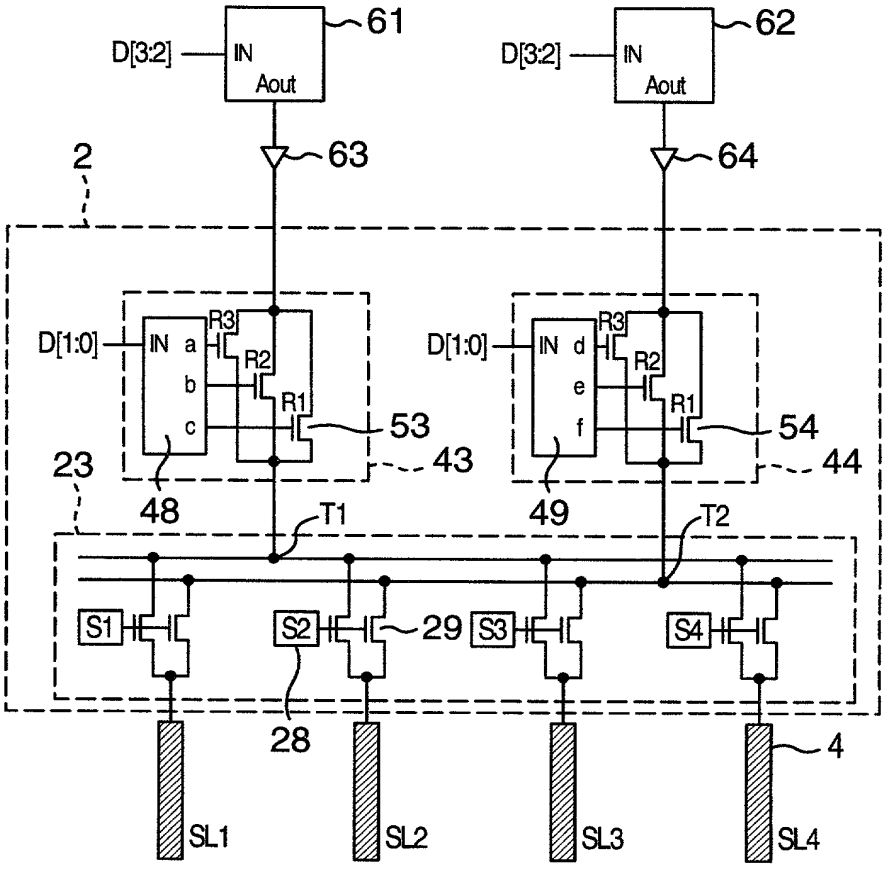


FIG. 11

IN	61 Aout	62 Aout
0	V0	V1
1	V1	V2
2	V2	V3
3	V3	V4

FIG. 12

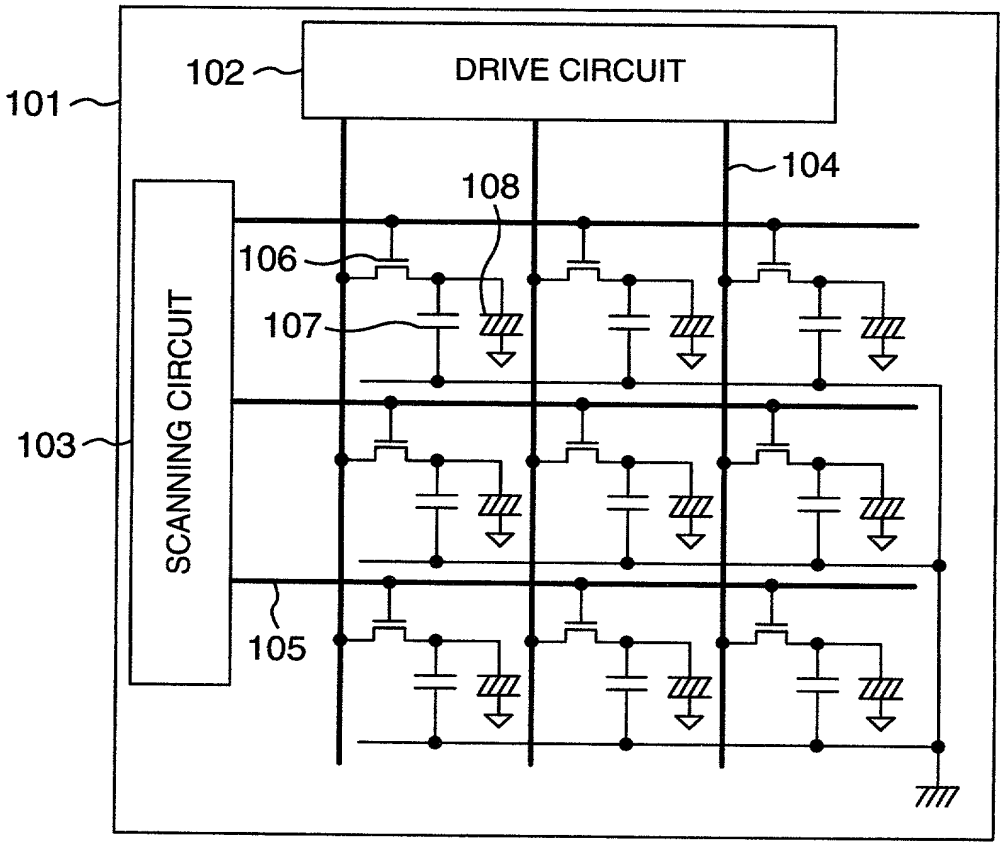

101
102
DRIVE CIRCUIT
104
108
106
107
SCANNING CIRCUIT
103
105

FIG. 13

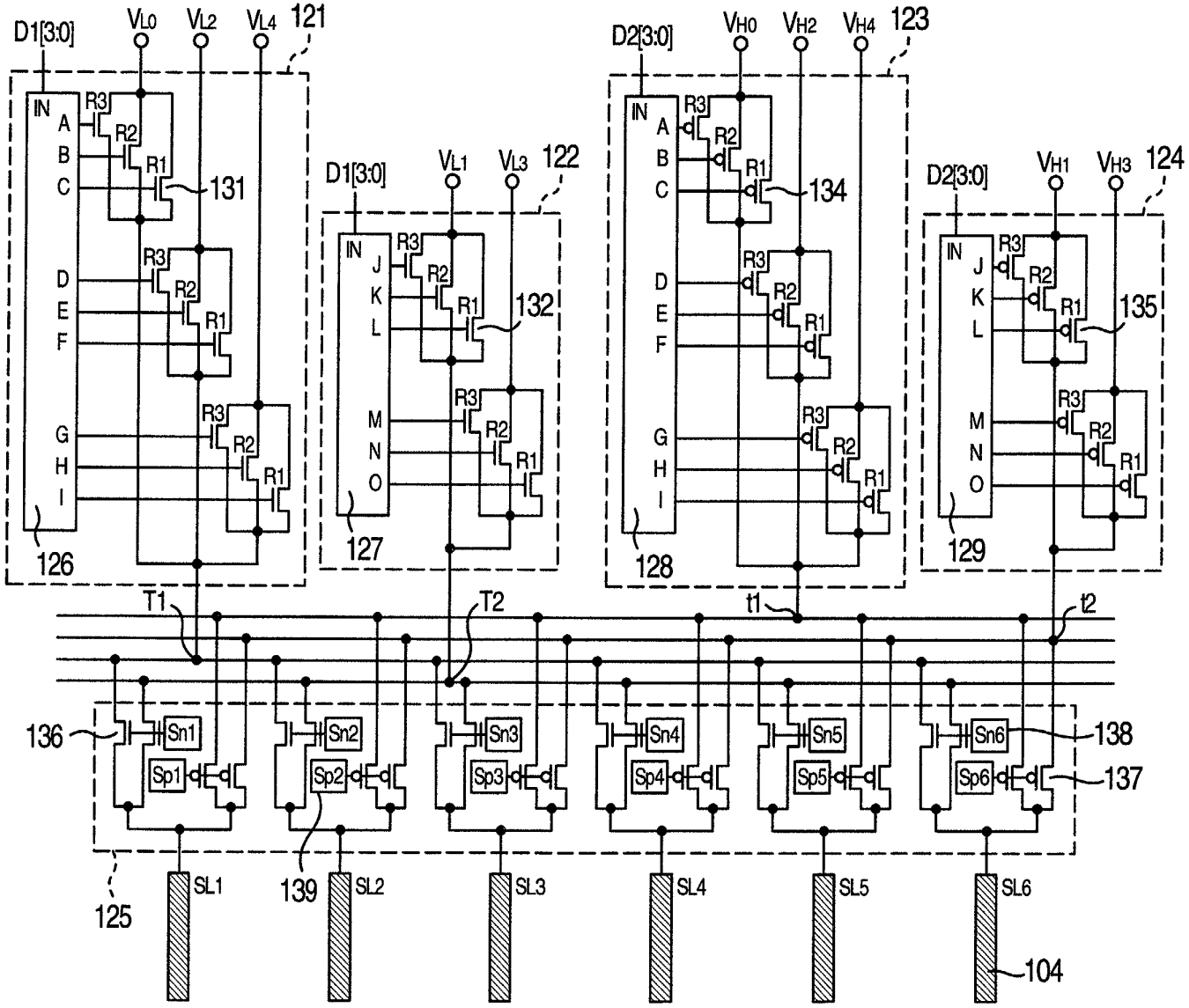

D1[3:0]
VL0
VL2
VL4
121
IN
A
B
C
D
E
F
G
H
I
R3
R2
R1
131
126
D1[3:0]
VL1
VL3
122
J
K
L
M
N
O
132
127
D2[3:0]
VH0
VH2
VH4
123
134
128
D2[3:0]
VH1
VH3
124
135
129
T1
T2
t1
t2
136
Sn1
Sn2
Sn3
Sn4
Sn5
Sn6
Sp1
Sp2
Sp3
Sp4
Sp5
Sp6
138
137
125
139
SL1
SL2
SL3
SL4
SL5
SL6
104

FIG. 14A

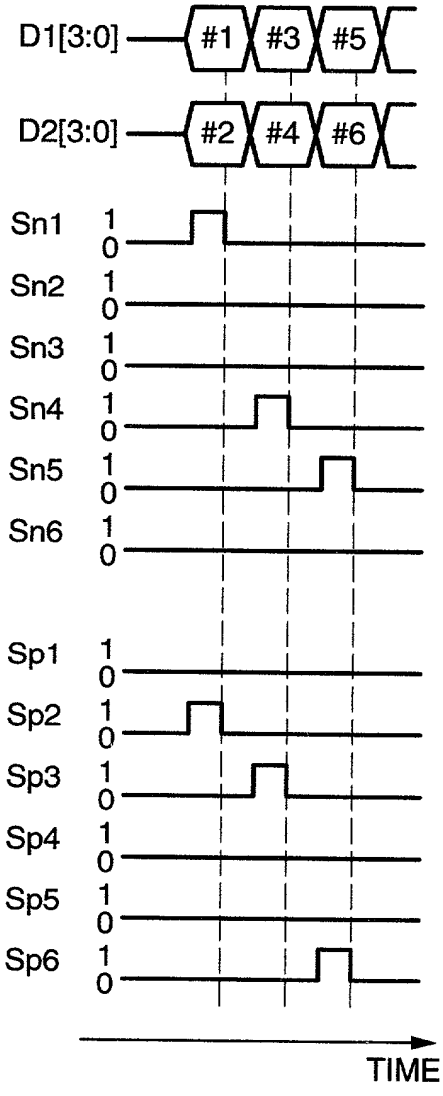


FIG. 14B

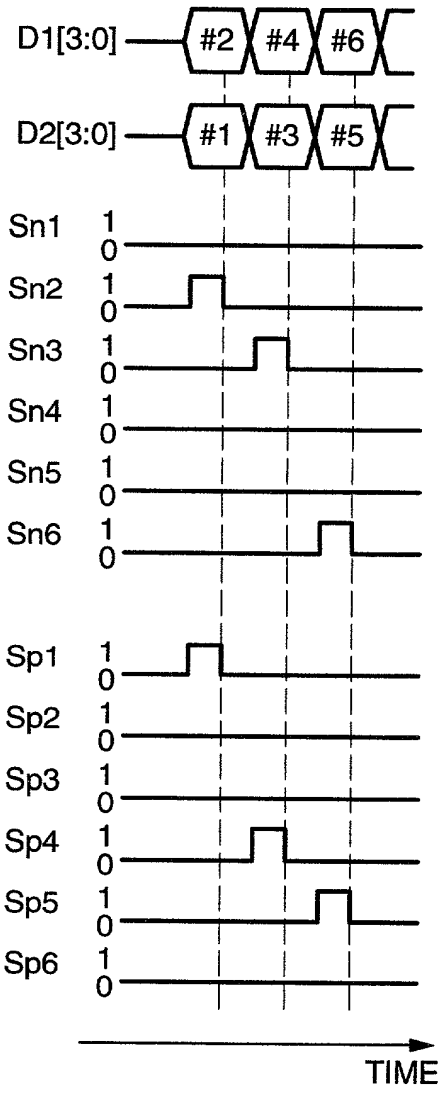


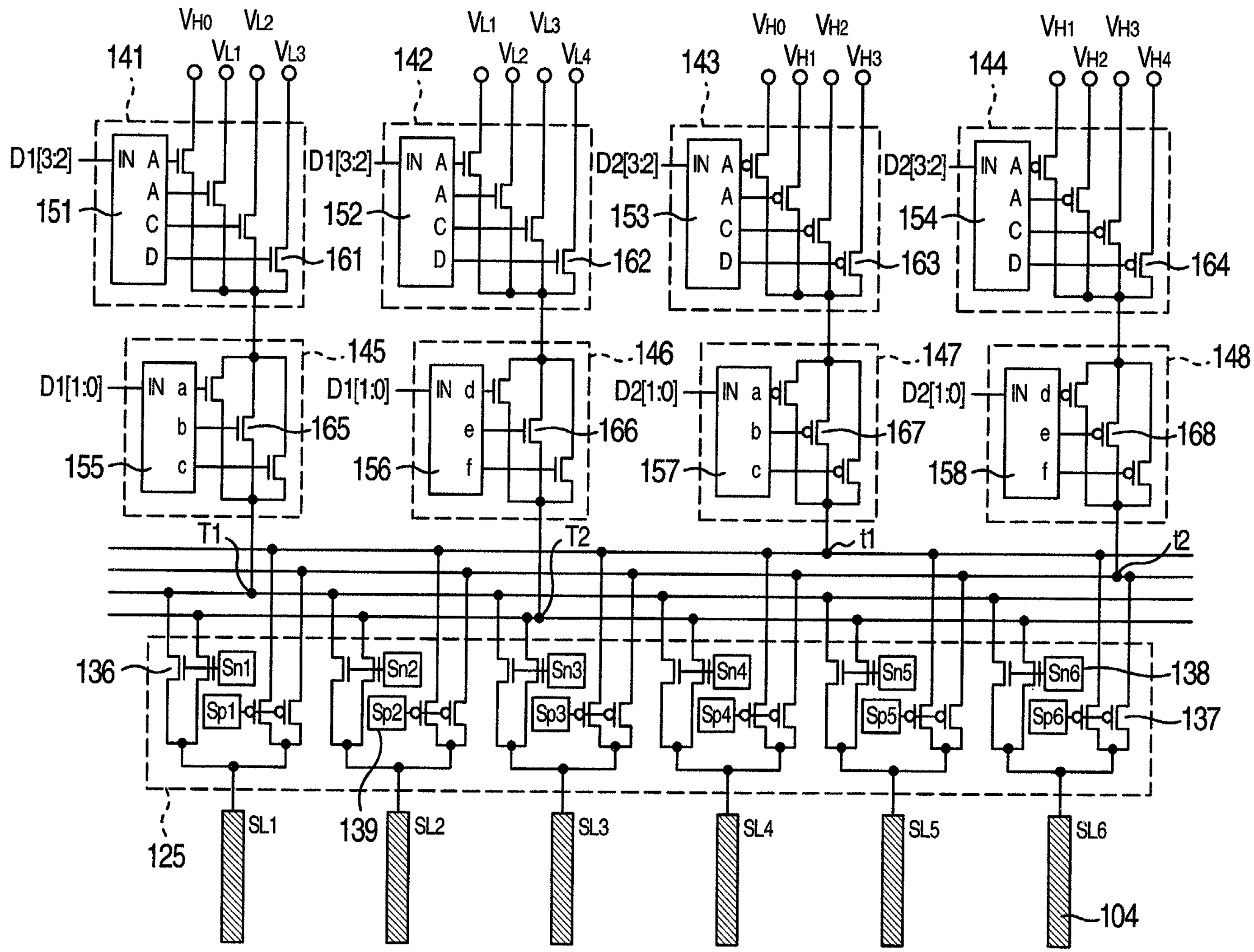
FIG. 15

D[3:0]	(a)	(b)
0	V_{H0}	V_{L0}
1	$(3V_{H0}+V_{H1})/4$	$(3V_{L0}+V_{L1})/4$
2	$(V_{H0}+V_{H1})/2$	$(V_{L0}+V_{L1})/2$
3	$(V_{H0}+3V_{H1})/4$	$(V_{L0}+3V_{L1})/4$
4	V_{H1}	V_{L1}
5	$(3V_{H1}+V_{H2})/4$	$(3V_{L1}+V_{L2})/4$
6	$(V_{H1}+V_{H2})/2$	$(V_{L1}+V_{L2})/2$
7	$(V_{H1}+3V_{H2})/4$	$(V_{L1}+3V_{L2})/4$
8	V_{H2}	V_{L2}
9	$(3V_{H2}+V_{H3})/4$	$(3V_{L2}+V_{L3})/4$
10	$(V_{H2}+V_{H3})/2$	$(V_{L2}+V_{L3})/2$
11	$(V_{H2}+3V_{H3})/4$	$(V_{L2}+3V_{L3})/4$
12	V_{H3}	V_{L3}
13	$(3V_{H3}+V_{H4})/4$	$(3V_{L3}+V_{L4})/4$
14	$(V_{H3}+V_{H4})/2$	$(V_{L3}+V_{L4})/2$
15	$(V_{H3}+3V_{H4})/4$	$(V_{L3}+3V_{L4})/4$

FIG. 18

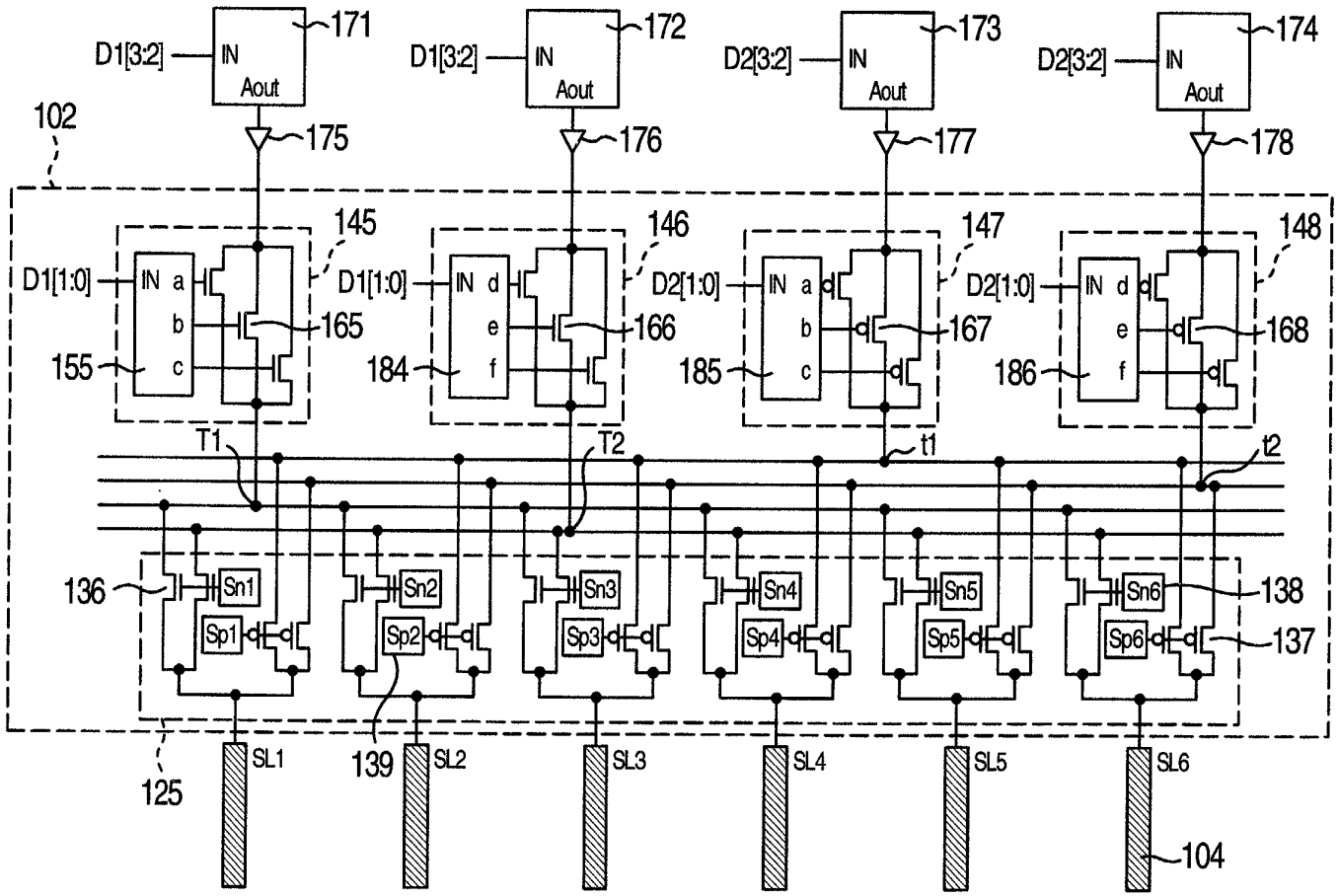
IN	171About	172About	173About	174About
0	VL0	VL1	VH0	VH1
1	VL1	VL2	VH1	VH2
2	VL2	VL3	VH2	VH3
3	VL3	VL4	VH3	VH4

FIG. 16



VH0
VL1
VL2
VL3
VL4
VH1
VH2
VH3
VH4
141
142
143
144
145
146
147
148
D1[3:2]
D2[3:2]
D1[1:0]
D2[1:0]
IN
A
C
D
a
b
c
d
e
f
151
152
153
154
155
156
157
158
161
162
163
164
165
166
167
168
T1
T2
t1
t2
136
137
138
139
125
Sn1
Sn2
Sn3
Sn4
Sn5
Sn6
Sp1
Sp2
Sp3
Sp4
Sp5
Sp6
SL1
SL2
SL3
SL4
SL5
SL6
104

FIG. 17


D1[3:2]
IN
Aout
171
172
173
174
D2[3:2]
102
175
176
177
178
145
146
147
148
D1[1:0]
D2[1:0]
IN a
b
c
d
e
f
155
184
185
186
165
166
167
168
T1
T2
t1
t2
136
138
137
Sn1
Sn2
Sn3
Sn4
Sn5
Sn6
Sp1
Sp2
Sp3
Sp4
Sp5
Sp6
125
139
SL1
SL2
SL3
SL4
SL5
SL6
104